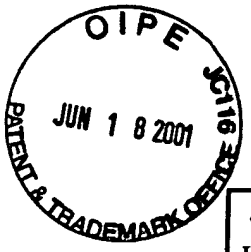

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ATTENUATING UNDESIRED FREQUENCIES WHILE SAMPLING A COMMUNICATION SIGNAL

This application claims the priority under 35 U.S.C. 119(e)(1) of copending U.S. provisional application number 60/204,902 filed on May 15, 2000.

FIELD OF THE INVENTION

The invention relates generally to frequency channel communications and, more particularly, to attenuation of undesired frequencies in frequency channel communications.

BACKGROUND OF THE INVENTION

In communications applications that utilize frequency channels, for example, wireless and wired RF communications, the energy in the desired frequency channel can be much lower than the energy in adjacent, undesired frequency channels. Accordingly, in order to extract communication signals from the desired frequency channel, communication receiver architectures must address the interference caused by adjacent frequency channels, particularly those of higher energy than the desired frequency channel.

Some conventional RF receiver architectures, such as super-heterodyne and direct conversion architectures, utilize high "Q" band-pass SAW filters (channel select filters)

to attenuate the interferers. Such filters produce a relatively clean channel signal that can then be converted to digital format using conventional low-resolution analog-to-digital converters (ADCs). However, these filters are typically ceramic or crystal electromechanical filters which are disadvantageously large and costly, and which impose an undesirably large signal power loss.

In highly integrated communication systems, direct conversion architectures are typically preferred because they permit elimination of SAW filters and hence component count reduction. These architectures also permit the desired channel selection to be performed in the digital domain using digital filters. An exemplary direct conversion architecture is illustrated diagrammatically in FIGURE 1. The RF communication signal is mixed down at 11, and applied to an anti-aliasing filter at 13. The output of the anti-aliasing filter 13 is applied to a high frequency analog-to-digital converter (e.g., a $\Delta\Sigma$ modulator) 15. The analog-to-digital converter (ADC) works at a selected sampling rate to digitize the entire frequency band including the interferers. The interferers are then attenuated by digital filtering at 17. The respective signal outputs from each of the components 11, 13, 15 and 17 are also graphically illustrated in FIGURE 1.

Direct conversion architectures provide high integration capability by trading off analog filter complexity (eliminating the external analog SAW filter) for increases in the oversampling rate and dynamic range of the ADC. One advantage of this approach is the cost reduction due to elimination of external components, but the drawback is, in general, increased power consumption. The increased dynamic range requirement of the ADC is

due to the higher interferer energy (relative to the desired signal) caused by the relaxed front-end filter.

Moreover, high linearity is needed in order to keep intermodulation products out of the desired frequency band. For example, in GSM systems, more than 80 dB is needed in a 135 KHz band and, in 3rd generation wireless systems, nearly 80 dB is needed in a 2 MHz bandwidth. Thus, the required ADC design is very challenging, and disadvantageously consumes large amounts of power. Another disadvantage of direct conversion architectures is that, because the interferers are converted into digital format together with the desired signal, any gain provided by automatic gain control (AGC) is also applied to the interferers.

It is therefore desirable to provide for attenuation of interfering frequency channels without the aforementioned disadvantages of the conventional approaches.

The invention incorporates switched capacitor filtering into the process of sampling the analog signal at the input of the ADC. Merging the switched capacitor filter with the ADC advantageously eliminates the need for a large, costly analog filter, while still avoiding complicated ADC design features described above.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 diagrammatically illustrates an example of a conventional direct conversion receiver architecture.

FIGURE 2 diagrammatically illustrates pertinent portions of exemplary embodiments of a communication receiver according to the invention.

FIGURE 3 diagrammatically illustrates pertinent portions of FIGURE 2 in more detail.

FIGURE 4 illistrates an exemplary embodiment of a filter bank of FIGURE 3.

FIGURE 5 graphically illustrates an exemplary impulse response associated with the filter bank of FIGURE 4.

FIGURE 6 graphically illustrates an impulse response of an exemplary filter bank according to the invention.

FIGURE 7 graphically illustrates the frequency response of a filter bank having the impulse response of FIGURE 6.

FIGURE 8 graphically illustrates the impulse response of another exemplary filter bank according to the invention.

FIGURE 9 graphically illustrates the frequency response of a filter bank having the impulse response of FIGURE 8.

FIGURE 10 illustrates exemplary operations which can be performed by the embodiments of FIGURES 2-4.

DETAILED DESCRIPTION

FIGURE 2 diagrammatically illustrates pertinent portions of exemplary embodiments of a communication receiver (e.g., GSM or CDMA) according to the invention. A baseband portion of the communication receiver example of FIGURE 2 includes an ADC 23 (e.g. a $\Delta\Sigma$ modulator) coupled to receive an analog input from, for example, an anti-aliasing filter such as illustrated at 13 in FIGURE 1. The ADC 23 is coupled to a switched capacitor filter bank (or a plurality of such filter banks) at 21. The filter bank 21 is also coupled to receive the output of the anti-aliasing filter 13. The switched capacitor filter bank 21 is cooperable with the ADC 23 for attenuating interferers in conjunction with the sampling operation of the ADC 23. Thus, in the digitized output 24 of the ADC 23, the interfering frequencies have been attenuated by operation of the switched capacitor filter bank 21. The signal 24, containing digitized information indicative of the desired communication on the desired frequency channel, is applied to a digital processing section 25 which can process the signal, for example, in any desired conventional manner.

FIGURE 3 diagrammatically illustrates pertinent portions of exemplary embodiments of the ADC 23 of FIGURE 2. In particular, FIGURE 3 illustrates one example of a single ended input sampling network for a switched capacitor circuit. The switches S1 and S2 are controlled by a switch controller 33 for sampling the analog input signal V_{IN} by storing the associated charge in capacitor C_{IN}. Switches S3 and S4 are cooperable under control of the switch controller 33 for dumping the charge stored in

capacitor C_{IN} in order to drive an integrator 30 including an operational amplifier 35 and an integrating capacitor C_{INT}. The output 36 of the integrator is provided to further portions 37 of the ADC 23. These further portions are well known in the art, and are therefore not explicitly detailed in FIGURE 3. The switched capacitor arrangement at S1-S4 and C_{IN} in FIGURE 3 is also conventional (other standard arrangements could also be used), as is the integrator 30. According to the invention, the input signal V_{IN} is applied to the switched capacitor filter bank(s) 21 which provide(s) an output signal at a charge summing node 32 of modulator 23.

FIGURE 4 illustrates an exemplary embodiment of a switched capacitor filter bank 21 according to the invention. The filter bank example of FIGURE 4 includes five sections designated generally by K0, K1, K2, K3 and K4. Each of these sections includes an associated pair of switches, $S1_{K0}$ and $S3_{K0}$, $S1_{K1}$ and $S3_{K1}$, etc. Each of the switch pairs of FIGURE 4 corresponds operationally with the switch pair S1 and S3 in FIGURE 3. For example, switch $S1_{K0}$ of FIGURE 4 cooperates with switch S2 of FIGURE 3 to sample the input signal V_{IN} by storing charge in capacitor C_{K0}. Also, the switch $S3_{K0}$ of FIGURE 4 cooperates with the switch S4 of FIGURE 3 for dumping charge from the capacitor C_{K0} to drive the integrator 30. The switch pairs of the remaining sections K1 through K4 of FIGURE 4 also cooperate with switches S2 and S4 of FIGURE 3 to perform sample and dump operations analogous to those described above with respect to section K0.

The switches of FIGURE 4 are controlled by the switch controller 33 of FIGURE 3 so as to implement a finite impulse response (FIR) filter, for example a filter having the impulse response illustrated in FIGURE 5. In order to implement the filter characteristic illustrated in FIGURE 5, the switch controller 33 controls the switches of FIGURE 4 such that, during each sample and dump cycle performed by switches S1 – S4 of FIGURE 3, one of the switches $S1_{K0}$-$S1_{K4}$ of one of the filter sections of FIGURE 4 cooperates with switch S2 of FIGURE 3 to store charge (sample) in its associated capacitor, and one of the switches $S3_{K0}$-$S3_{K4}$ of another of the filter sections of FIGURE 4 cooperates with switch S4 of FIGURE 3 to dump charge from its associated capacitor.

A specific example of implementing the filter characteristic illustrated in FIGURE 5 is described in the following steps (1) – (5). (1) During a given sample operation by switches S1 and S2 of FIGURE 3, switch $S1_{K0}$ of FIGURE 4 also cooperates with switch S2 of FIGURE 3 to sample the input signal V_{IN} at capacitor C_{K0}. Thereafter, during the corresponding (immediately following) dump operation performed by switches S3 and S4 of FIGURE 3, switch $S3_{K1}$ of FIGURE 4 cooperates with switch S4 of FIGURE 3 to dump the charge from capacitor C_{K1} while the charge from capacitor C_{IN} of FIGURE 3 is also being dumped via switches S3 and S4 of FIGURE 3. (2) During the next sample operation of switches S1 and S2 of FIGURE 3, switch $S1_{K1}$ of FIGURE 4 cooperates with switch S2 of FIGURE 3 to perform a sample operation with respect to capacitor C_{K1}. During the corresponding (immediately following) dump operation performed by switches S3 and S4 of FIGURE 3, switch $S3_{K2}$ of FIGURE 4 cooperates with switch S4

of FIGURE 3 to dump the charge from capacitor C_{K2}. (3) During the next sample operation of switches S1 and S2 of FIGURE 3, switch $S1_{K2}$ of FIGURE 4 cooperates with swtich S2 of FIGURE 3 to perform a sample operation with respect to capicitor C_{K2}. During the corresponding (immediately following) dump operation performed by switches S3 and S4 of FIGURE 3, switch $S3_{K3}$ of FIGURE 4 cooperates with switch S4 of FIGURE 3 to dump the charge from capacitor C_{K3}. (4) During the next sample operation of switches S1 and S2 of FIGURE 3, switch $S1_{K3}$ of FIGURE 4 cooperates with switch S2 of FIGURE 3 to perform a sample operation with respect to capacitor C_{K3}. During the corresponding (immediately following) dump operation performed by switches S3 and S4 of FIGURE 3, switch $S3_{K4}$ of FIGURE 4 cooperates with switch S4 of FIGURE 3 to dump the charge from capacitor C_{K4}. (5) During the next sample operation of switches S1 and S2 of FIGURE 3, switch $S1_{K4}$ of FIGURE 4 cooperates with switch S2 of FIGURE 3 to perform a sample operation with respect to capacitor C_{K4}. During the corresponding (immediately following) dump operation performed by switches S3 and S4 of FIGURE 3, switch $S3_{K0}$ of FIGURE 4 cooperates with switch S4 of FIGURE 3 to dump the charge from capacitor C_{K0}.

During the next sample operation of switches S1 and S2 of FIGURE 3, switch $S1_{K0}$ of FIGURE 4 again cooperates with switch S2 of FIGURE 3 to perform another sample operation with respect to capacitor C_{K0}, whereby it can be seen that step (1) above is performed again, and steps (1) – (5) are repeated.

As above-described operations (1) – (5) demonstrate, in general, one or more capacitors can be charged at the same time, and the charge from one or more capacitors can be dumped at the same time during a given dump phase.

The above-described operation of the filter bank of FIGURE 4 in response to the switch controller 33 causes the charge corresponding to the (i–4)th sample (input that was sampled four clock periods before the current period) to be dumped from a capacitor in FIGURE 4 in parallel with the dumping of the charge corresponding to the ith (current) sample from capacitor C_{IN} of FIGURE 3. This operation implements the filter characteristic of FIGURE 5.

As indicated above, a plurality of filter banks can be provided at 21 in order to provide an FIR filter having any desired number of taps. As shown in FIGURES 4 and 5, the filter bank(s) at 21 can implement very simple FIRs that can be used to attenuate the desired interferer at the desired frequency. Undesirable phase distortion can be avoided by using linear phase FIR filters, such as illustrated in FIGURE 4. The capacitors in the filter bank(s), for example capacitors $C_{K0} – C_{K4}$ can of course be scaled to produce the desired filter characteristics. Such capacitor scaling in order to obtain a desired filter characteristic is well known in the art of switched capacitor filter design.

An automatic gain control (AGC) function can be easily provided, for example, by switching the integrating capacitor C_{INT} in FIGURE 3 from one value to another, thereby effectively scaling the signal. Because this signal scaling occurs after the

interferers have been attenuated by the filter at 21, distortion is reduced in the integrator output 36.

The exemplary bank of capacitors in FIGURE 4 can implement one or more FIR responses, depending on the operation of the switch controller 33 of FIGURE 3. Different FIR responses can implement different filters, or also different scalings of the same filter. The FIR filter to be implemented determines which capacitors will be used for sampling and which capacitors will be used for dumping in each cycle. Using straightforward digital design techniques, the switch controller 33 can be designed to implement the switching sequence necessary to produce the desired FIR response.

In some embodiments, the switched capacitor filter 21 can be designed together with the anti-aliasing filter 13 (see also FIGURE 1) to provide optimization of the overall performance. The goal of this optimization is to attenuate the interferers according to the communication channel specifications while minimizing the power consumption in the analog anti-aliasing filter, the FIR filter, and the ADC.

According to another exemplary feature of the present invention, FIR filters with negative coefficients can be readily obtained in differential implementations by cross-coupling those capacitors which sample the positive input such that they are dumped to the negative summing node, and vice versa.

FIGURE 6 graphically illustrates the impulse response of an exemplary switched capacitor FIR filter according to the invention. The filter characteristic of FIGURE 6 is suitable, for example, for use in a communication receiver in a GSM system. FIGURE 7

graphically illustrates the performance associated with the filter characteristic of FIGURE 6. The curve at 71 illustrates the performance when only the FIR filter of FIGURE 6 is utilized, and the curve at 72 illustrates the performance when the FIR filter characteristic of FIGURE 6 is combined with a third order anti-aliasing filter. The curve 72 demonstrates better than 25 dB rejection of interferers.

FIGURE 8 graphically illustrates the impulse response of another exemplary switched capacitor FIR filter according to the invention. The filter characteristic of FIGURE 8 is suitable, for example, for use in communication receivers operating in WCDMA systems. FIGURE 9 graphically illustrates the performance obtained using the filter characteristic of FIGURE 8 with a third order anti-aliasing filter (92) and with the filter of FIGURE 8 only (91).

FIGURE 10 illustrates exemplary operations which can be performed by the communication receiver embodiments of FIGURES 2-4. At 101, the analog signal, including interferers, is received. At 102, the above-described sampling operation, incorporating the filter function for removing the interferers, is performed. At 103, the result of the sampling operation is provided (dumped) for conversion to digital format.

It should be clear from the foregoing description that the present invention provides a highly linear, low power technique for filtering out-of-band interferers, while still enabling a fully integrated communication receiver by eliminating external filter components. By filtering the out-of-band interference before conversion of the signal into digital format, the design complexity of the ADC is reduced as compared to prior art

arrangements wherein all of the interferers are converted into digital format and then filtered digitally. The invention can utilize a simple, passive FIR switched capacitor network (merged with the functionality of the ADC) with a very small number of non-zero coefficients, and the filter can be optimized to produce band-stop regions in alignment with the most critical interferers. This enables the use of ADCs having a dynamic range that is lower by more than 12 to 20 dB relative to ADCs used in direct conversion receivers. Such lower dynamic range ADCs have lower size and power requirements, and also require less noise isolation. The small number of non-zero coefficients in the FIR filter, and its application at the sampling input of the ADC provide for a simple implementation. It can be shown that simple integer ratios for the non-zero coefficients provides still more reductions in the size and dynamic range required by the ADC. Moreover, by simply altering the switch control applied to the FIR filter bank, the filter can be programmed to meet different band requirements as needed. This is particularly useful for multi-mode transceiver designs, and can also permit ADCs and filters to be shared between bands, thereby reducing the overall cost. Significant power reduction results from merging the FIR filter as part of the input stage of a switched capacitor ADC ($\Delta\Sigma$, piplined or any other ADC that has a single stage at its input to perform the sampling function). The first stage of such converters is the critical stage for linearity and signal-to-noise performance. The invention re-uses this first stage for the FIR function, and also re-uses the ADC's integrator (see 30 in FIGURE 3) to complete the realization of the filter, thereby advantageously achieving power reductions.

Although exemplary embodiments of the invention have been described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.